

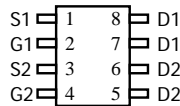
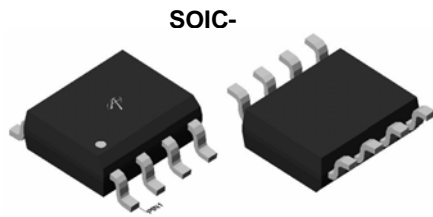
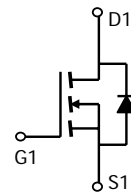
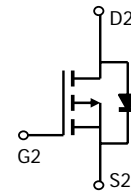
AO4622
Complementary Enhancement Mode Field Effect Transistor
General Description

The AO4622/L uses advanced trench technology MOSFETs to provide excellent $R_{DS(ON)}$ and low gate charge. The complementary MOSFETs may be used to form a level shifted high side switch, and for a host of other applications. AO4622 and AO4622L are electrically identical.

-RoHS Compliant
 -AO4622L is Halogen Free

Features

n-channel	p-channel
$V_{DS} (V) = 20V$	-20V
$I_D = 7.3A (V_{GS}=4.5V)$	-5A ($V_{GS}=-4.5V$)
$R_{DS(ON)}$	$R_{DS(ON)}$
< 23m Ω ($V_{GS}=10V$)	< 53m Ω ($V_{GS} = -4.5V$)
< 30m Ω ($V_{GS}=4.5V$)	< 87m Ω ($V_{GS} = -2.5V$)
< 84m Ω ($V_{GS}=2.5V$)	


SOIC-8

n-channel

p-channel
Absolute Maximum Ratings $T_A=25^\circ C$ unless otherwise noted

Parameter	Symbol	Max n-channel	Max p-channel	Units
Drain-Source Voltage	V_{DS}	20	-20	V
Gate-Source Voltage	V_{GS}	± 16	± 12	V
Continuous Drain Current ^{AF}	I_D	$T_A=25^\circ C$	-5	A
		$T_A=70^\circ C$	-4.2	
Pulsed Drain Current ^B	I_{DM}	35	-25	A
Power Dissipation	P_D	$T_A=25^\circ C$	2	W
		$T_A=70^\circ C$	1.44	
Avalanche Current ^B	I_{AR}	13	13	A
Repetitive avalanche energy 0.3mH ^B	E_{AR}	25	25	mJ
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	-55 to 150	$^\circ C$

Thermal Characteristics: n-channel and p-channel

Parameter	Symbol	Device	Typ	Max	Units	
Maximum Junction-to-Ambient ^A	$t \leq 10s$	$R_{\theta JA}$	n-ch	48	62.5	$^\circ C/W$
			n-ch	74	110	$^\circ C/W$
Maximum Junction-to-Lead ^C	Steady-State	$R_{\theta JL}$	n-ch	35	40	$^\circ C/W$
Maximum Junction-to-Ambient ^A	$t \leq 10s$	$R_{\theta JA}$	p-ch	48	62.5	$^\circ C/W$
			p-ch	74	110	$^\circ C/W$
Maximum Junction-to-Lead ^C	Steady-State	$R_{\theta JL}$	p-ch	35	40	$^\circ C/W$

N-Channel Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D=250\mu\text{A}$, $V_{GS}=0\text{V}$	20			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=16\text{V}$, $V_{GS}=0\text{V}$ $T_J=55^\circ\text{C}$			1	uA
					5	
I_{GSS}	Gate-Body leakage current	$V_{DS}=0\text{V}$, $V_{GS}=\pm 16\text{V}$			100	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	0.6	1.25	2	V
$I_{D(ON)}$	On state drain current	$V_{GS}=4.5\text{V}$, $V_{DS}=5\text{V}$	35			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS}=10\text{V}$, $I_D=7.3\text{A}$ $T_J=125^\circ\text{C}$		19	23	m Ω
				28	33.6	
			$V_{GS}=4.5\text{V}$, $I_D=6.4\text{A}$		24	
		$V_{GS}=2.5\text{V}$, $I_D=2\text{A}$		67	84	m Ω
g_{FS}	Forward Transconductance	$V_{DS}=5\text{V}$, $I_D=7.3\text{A}$		17		S
V_{SD}	Diode Forward Voltage	$I_S=1\text{A}$		0.7	1	V
I_S	Maximum Body-Diode Continuous Current				3	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	$V_{GS}=0\text{V}$, $V_{DS}=10\text{V}$, $f=1\text{MHz}$		900	1100	pF
C_{oss}	Output Capacitance			162		pF
C_{rss}	Reverse Transfer Capacitance			105		pF
R_g	Gate resistance	$V_{GS}=0\text{V}$, $V_{DS}=0\text{V}$, $f=1\text{MHz}$		0.9	1.35	Ω
SWITCHING PARAMETERS						
$Q_g(10\text{V})$	Total Gate Charge	$V_{GS}=10\text{V}$, $V_{DS}=10\text{V}$, $I_D=6.5\text{A}$		15	18	nC
$Q_g(4.5\text{V})$	Total Gate Charge			7.2	9	nC
Q_{gs}	Gate Source Charge			1.8		nC
Q_{gd}	Gate Drain Charge			2.8		nC
$t_{D(on)}$	Turn-On Delay Time	$V_{GS}=10\text{V}$, $V_{DS}=10\text{V}$, $R_L=1.4\Omega$, $R_{GEN}=3\Omega$		4.5		ns
t_r	Turn-On Rise Time			9.2		ns
$t_{D(off)}$	Turn-Off Delay Time			18.7		ns
t_f	Turn-Off Fall Time			3.3		ns
t_{rr}	Body Diode Reverse Recovery Time	$I_F=7.3\text{A}$, $dI/dt=100\text{A}/\mu\text{s}$		18		ns
Q_{rr}	Body Diode Reverse Recovery Charge	$I_F=7.3\text{A}$, $dI/dt=100\text{A}/\mu\text{s}$		9.5		nC

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$. The value in any given application depends on the user's specific board design.

B: Repetitive rating, pulse width limited by junction temperature.

C: The $R_{\theta JA}$ is the sum of the thermal impedance from junction to lead $R_{\theta JL}$ and lead to ambient. $R_{\theta JL}$ and $R_{\theta JC}$ are equivalent terms referring to thermal resistance from junction to drain lead.

D: The static characteristics in Figures 1 to 6 are obtained using <300 μs pulses, duty cycle 0.5% max.

E: These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$. The SOA curve provides a single pulse rating.

F: The current rating is based on the $t \leq 10\text{s}$ thermal resistance rating.

Rev4: Nov 2008

THIS PRODUCT HAS BEEN DESIGNED AND QUALIFIED FOR THE CONSUMER MARKET. APPLICATIONS OR USES AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS ARE NOT AUTHORIZED. AOS DOES NOT ASSUME ANY LIABILITY ARISING OUT OF SUCH APPLICATIONS OR USES OF ITS PRODUCTS. AOS RESERVES THE RIGHT TO IMPROVE PRODUCT DESIGN, FUNCTIONS AND RELIABILITY WITHOUT NOTICE.

N-CHANNEL TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

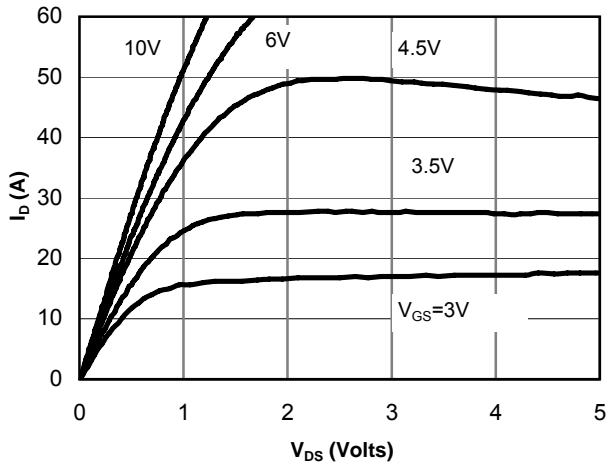


Figure 1: On-Region Characteristics

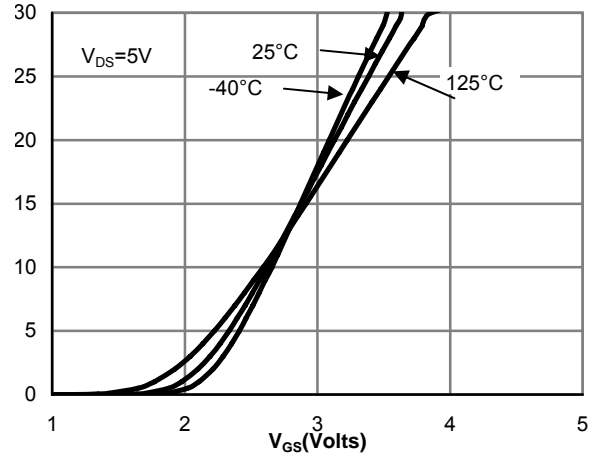


Figure 2: Transfer Characteristics

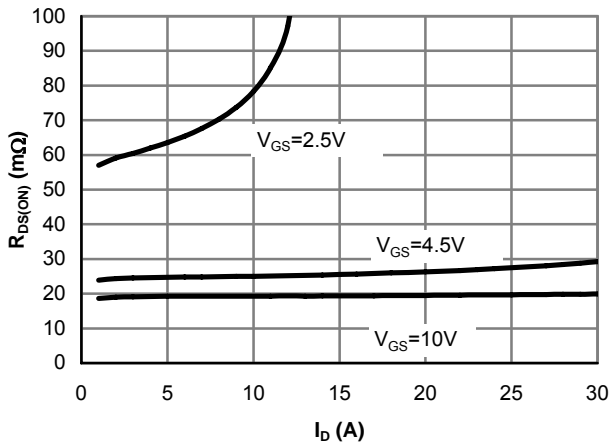


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

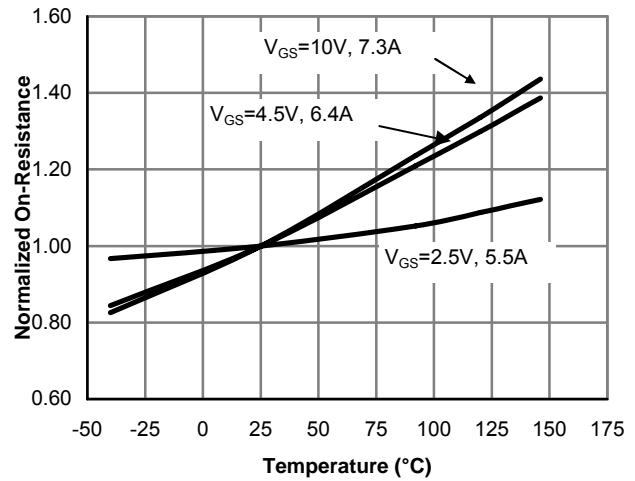


Figure 4: On-Resistance vs. Junction Temperature

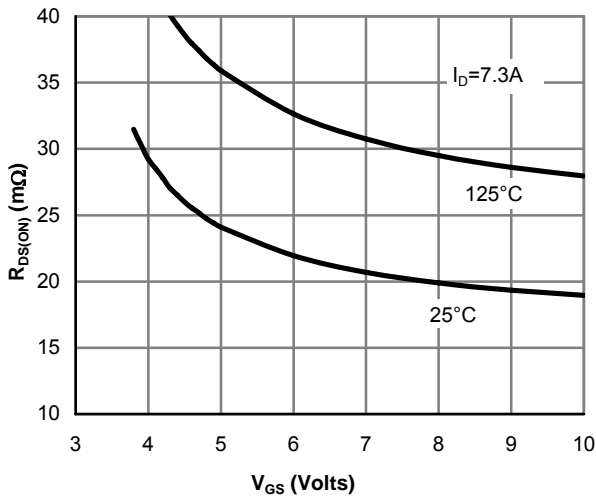


Figure 5: On-Resistance vs. Gate-Source Voltage

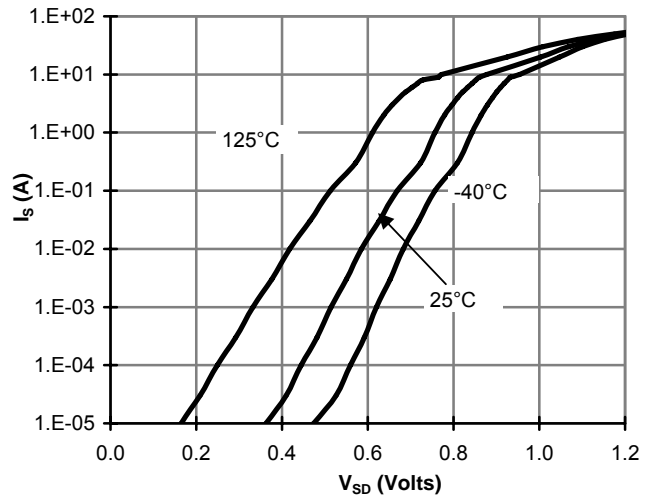


Figure 6: Body-Diode Characteristics

N-Channel TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

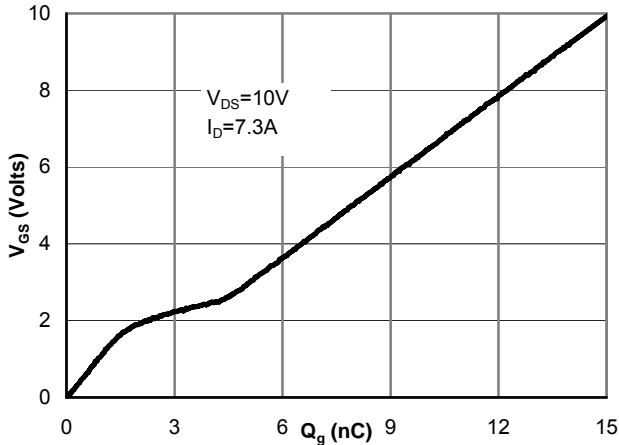


Figure 7: Gate-Charge Characteristics

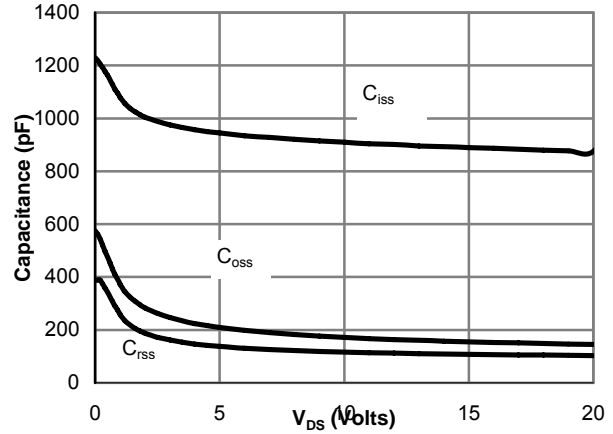


Figure 8: Capacitance Characteristics

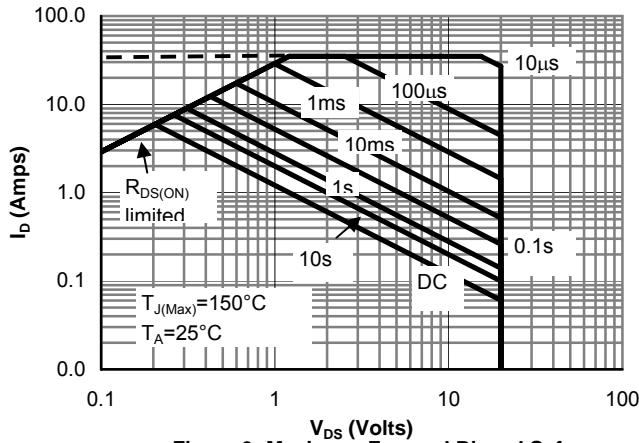


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

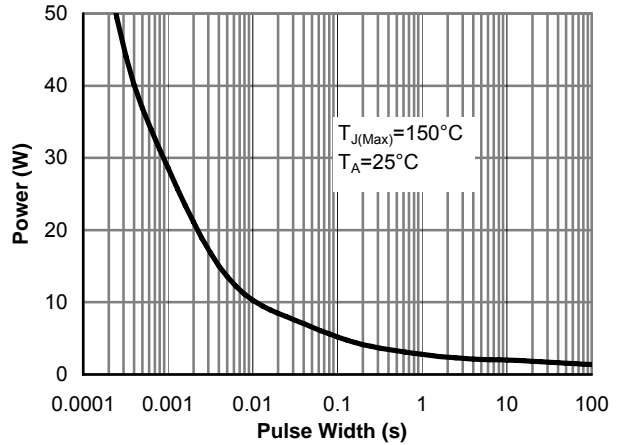


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

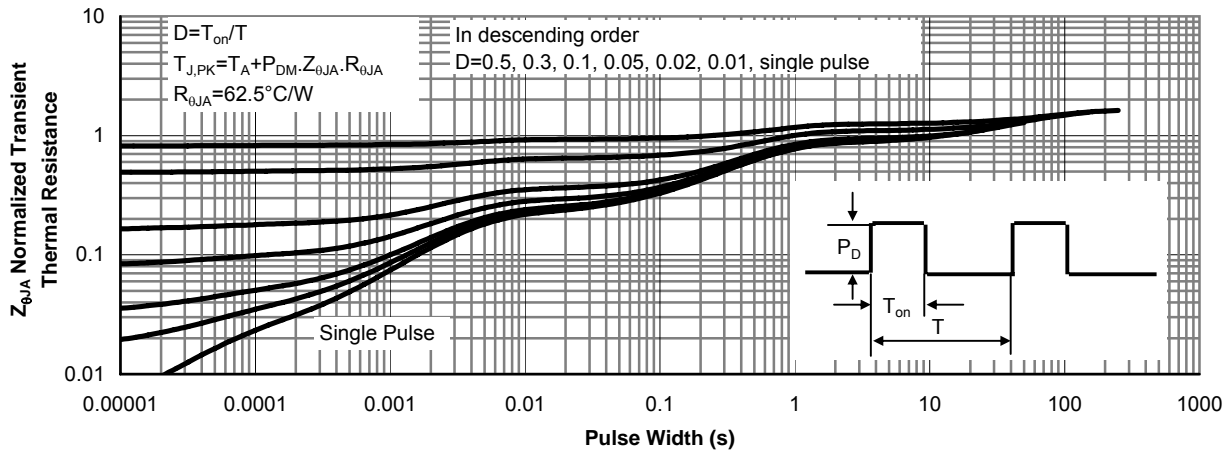
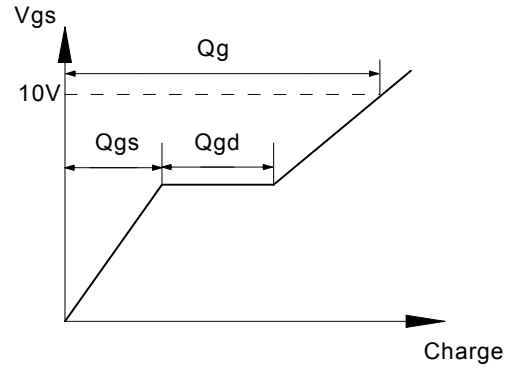
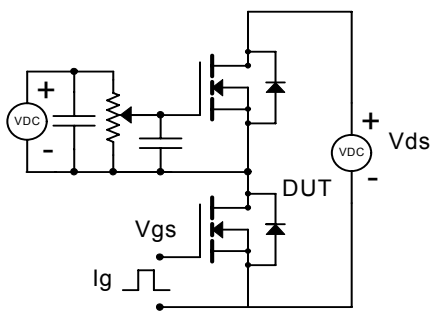
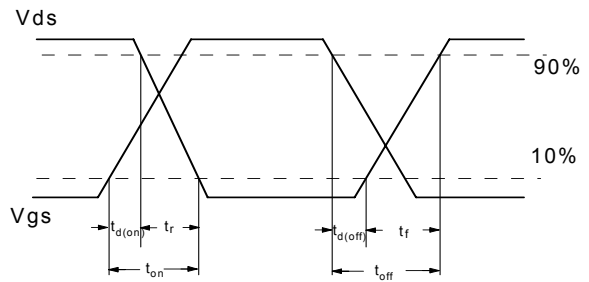
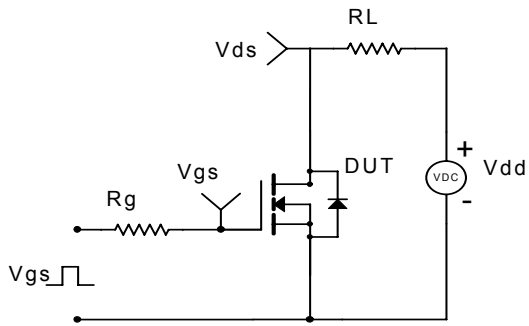


Figure 11: Normalized Maximum Transient Thermal Impedance

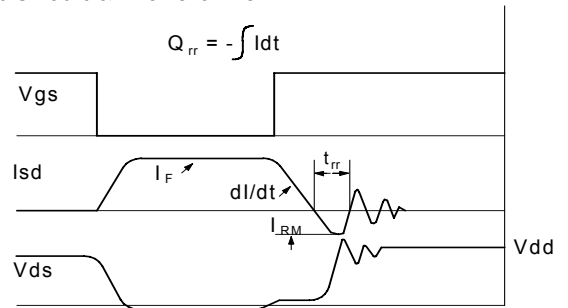
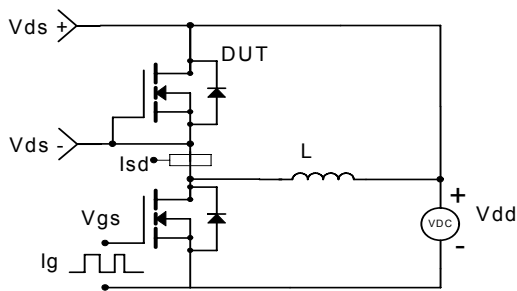
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



P-Channel Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D=-250\mu\text{A}$, $V_{GS}=0\text{V}$	-20			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=-16\text{V}$, $V_{GS}=0\text{V}$ $T_J=55^\circ\text{C}$			-1 -5	μA
I_{GSS}	Gate-Body leakage current	$V_{DS}=0\text{V}$, $V_{GS}=\pm 12\text{V}$			± 100	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$, $I_D=-250\mu\text{A}$	-1.3	-0.9	-0.5	V
$I_{D(ON)}$	On state drain current	$V_{GS}=-4.5\text{V}$, $V_{DS}=-5\text{V}$	-25			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS}=-4.5\text{V}$, $I_D=-5\text{A}$ $T_J=125^\circ\text{C}$		44	53	m Ω
		$V_{GS}=-2.5\text{V}$, $I_D=-4.2\text{A}$		59	71	
				67	87	m Ω
g_{FS}	Forward Transconductance	$V_{DS}=-5\text{V}$, $I_D=-5\text{A}$		13		S
V_{SD}	Diode Forward Voltage	$I_S=-1\text{A}$, $V_{GS}=0\text{V}$		-0.76	-1	V
I_S	Maximum Body-Diode Continuous Current				-2.5	A
DYNAMIC PARAMETERS						
C_{ISS}	Input Capacitance	$V_{GS}=0\text{V}$, $V_{DS}=-10\text{V}$, $f=1\text{MHz}$		800	960	pF
C_{OSS}	Output Capacitance			131		pF
C_{RSS}	Reverse Transfer Capacitance			103		pF
R_g	Gate resistance	$V_{GS}=0\text{V}$, $V_{DS}=0\text{V}$, $f=1\text{MHz}$		6.7	10	Ω
SWITCHING PARAMETERS						
$Q_g(10\text{V})$	Total Gate Charge (10V)	$V_{GS}=-4.5\text{V}$, $V_{DS}=-10\text{V}$, $I_D=-4.5\text{A}$		15.5		nC
$Q_g(4.5\text{V})$	Total Gate Charge (4.5V)			7.4		nC
Q_{gs}	Gate Source Charge			1.3		nC
Q_{gd}	Gate Drain Charge			2.9		nC
$t_{D(on)}$	Turn-On DelayTime			4.4		ns
t_r	Turn-On Rise Time	$V_{GS}=-4.5\text{V}$, $V_{DS}=-10\text{V}$, $R_L=2\Omega$, $R_{GEN}=3\Omega$		7.6		ns
$t_{D(off)}$	Turn-Off DelayTime			44		ns
t_f	Turn-Off Fall Time			13.5		ns
t_{rr}	Body Diode Reverse Recovery Time	$I_F=-5\text{A}$, $dI/dt=100\text{A}/\mu\text{s}$		20		ns
Q_{rr}	Body Diode Reverse Recovery Charge	$I_F=-5\text{A}$, $dI/dt=100\text{A}/\mu\text{s}$		9		nC

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$. The value in any given application depends on the user's specific board design.

B: Repetitive rating, pulse width limited by junction temperature.

C: The $R_{\theta JA}$ is the sum of the thermal impedance from junction to lead $R_{\theta JL}$ and lead to ambient. $R_{\theta JL}$ and $R_{\theta JC}$ are equivalent terms referring to thermal resistance from junction to drain lead.

D: The static characteristics in Figures 1 to 6 are obtained using <300 μs pulses, duty cycle 0.5% max.

E: These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$. The SOA curve provides a single pulse rating.

F: The current rating is based on the $t \leq 10\text{s}$ thermal resistance rating.

Rev4: Nov 2008

THIS PRODUCT HAS BEEN DESIGNED AND QUALIFIED FOR THE CONSUMER MARKET. APPLICATIONS OR USES AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS ARE NOT AUTHORIZED. AOS DOES NOT ASSUME ANY LIABILITY ARISING OUT OF SUCH APPLICATIONS OR USES OF ITS PRODUCTS. AOS RESERVES THE RIGHT TO IMPROVE PRODUCT DESIGN, FUNCTIONS AND RELIABILITY WITHOUT NOTICE.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS: P-CHANNEL

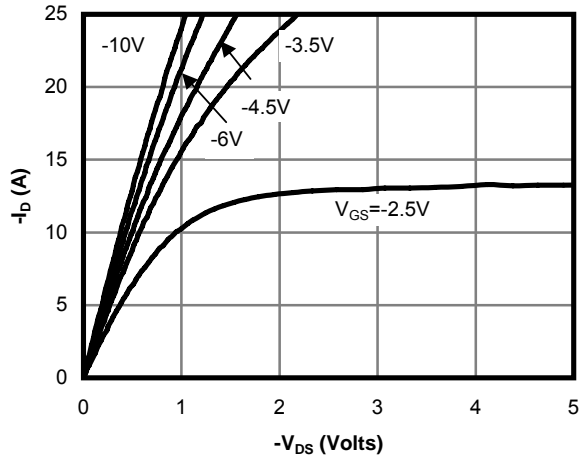


Fig 1: On-Region Characteristics

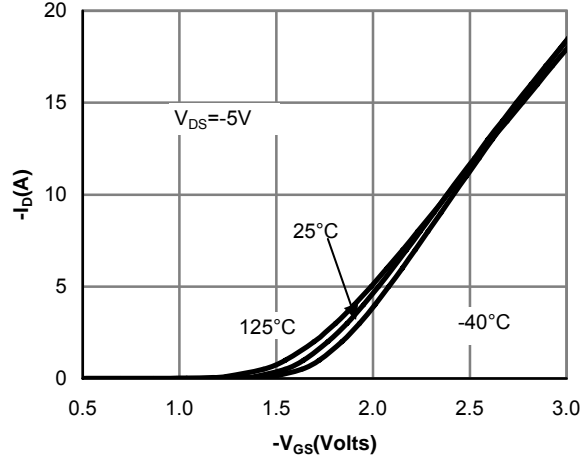


Figure 2: Transfer Characteristics

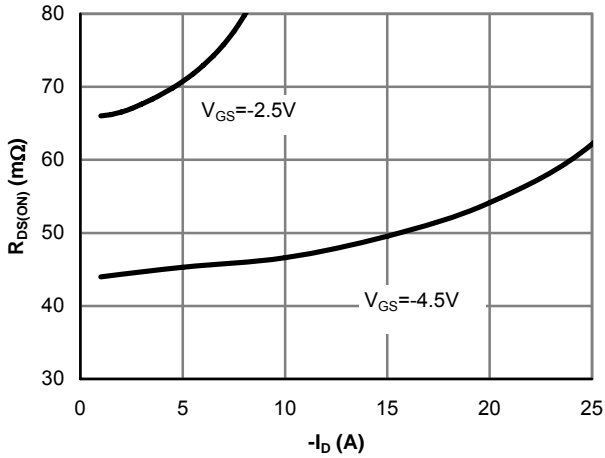


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

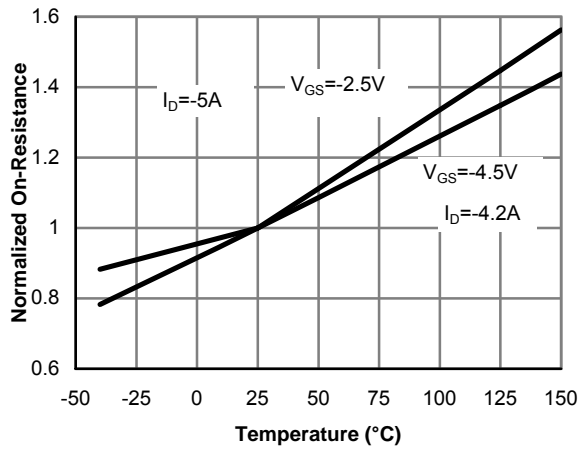


Figure 4: On-Resistance vs. Junction Temperature

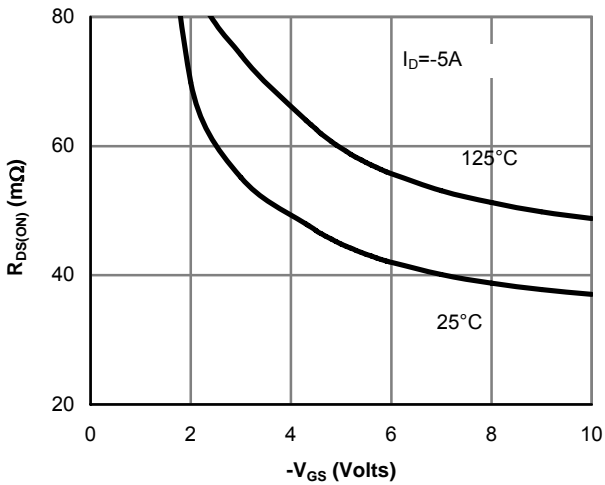


Figure 5: On-Resistance vs. Gate-Source Voltage

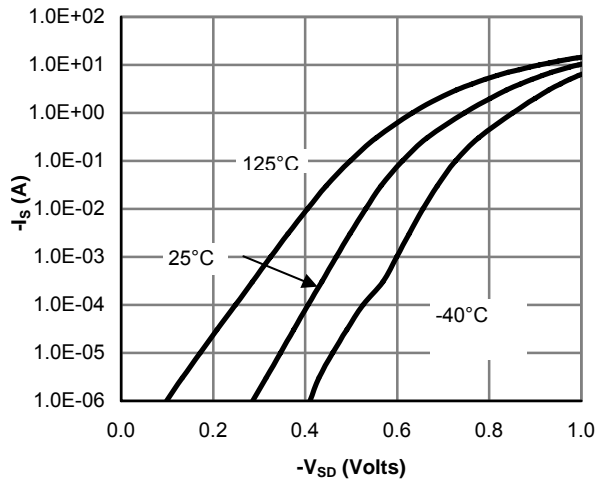


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS: P-CHANNEL

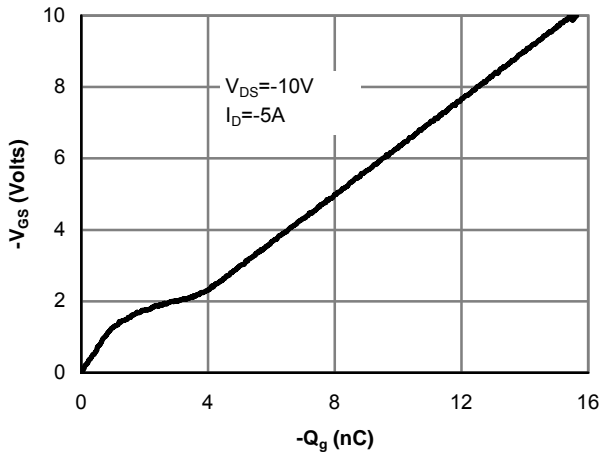


Figure 7: Gate-Charge Characteristics

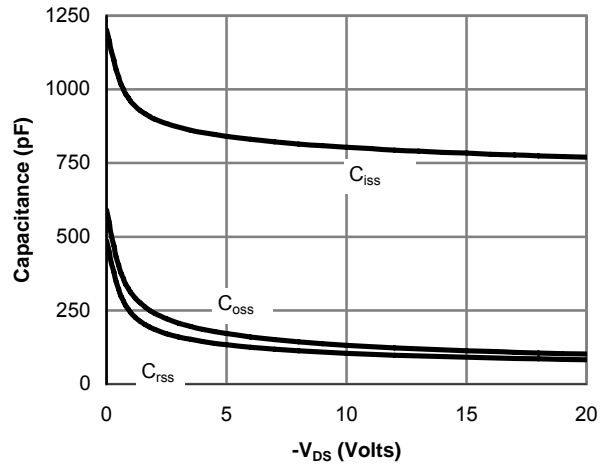


Figure 8: Capacitance Characteristics

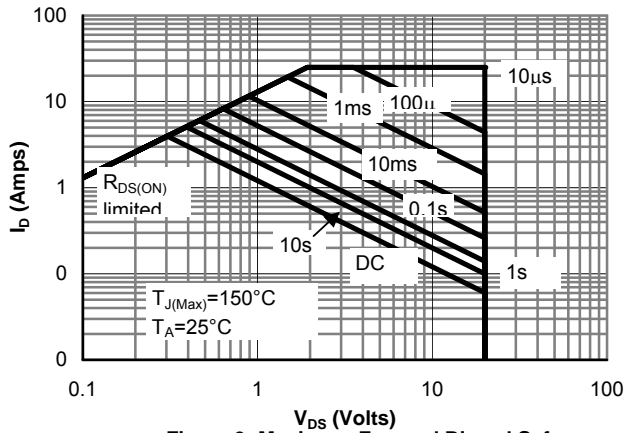


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

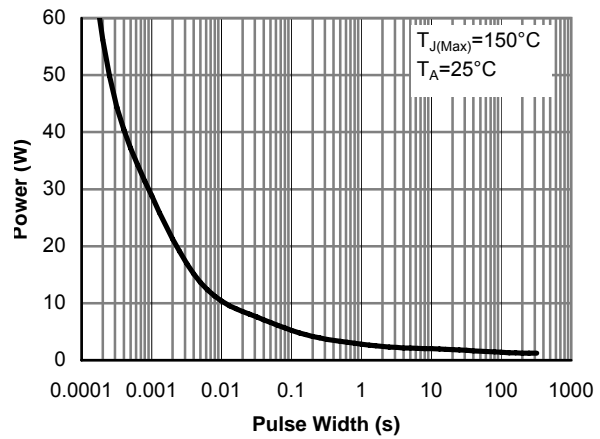


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

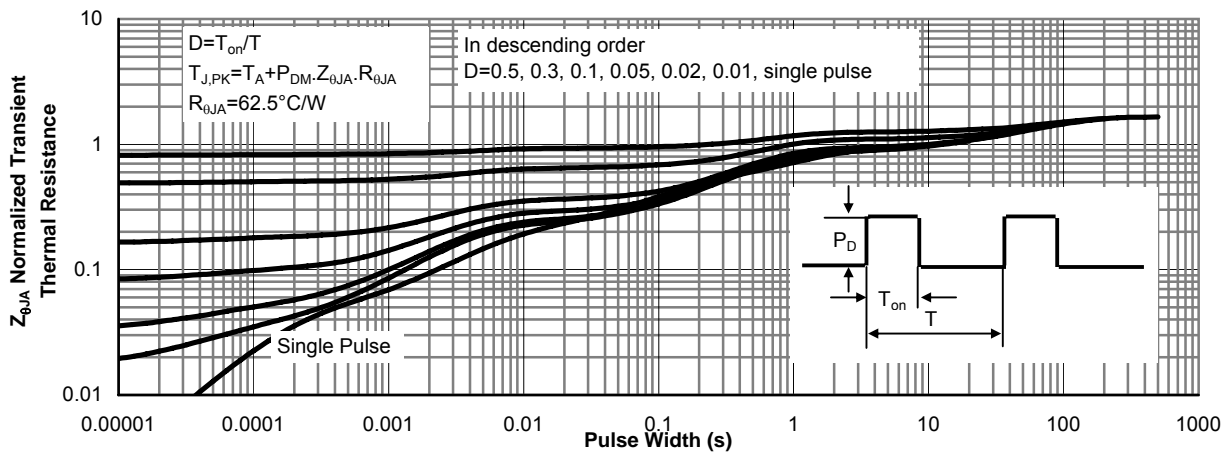
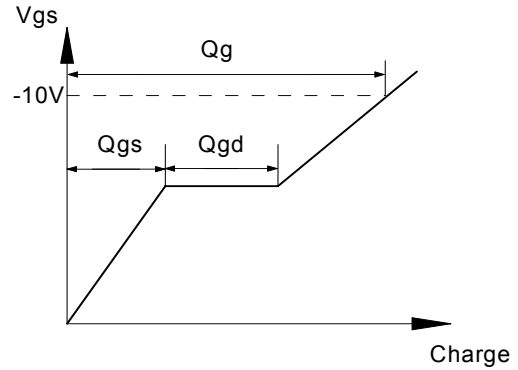
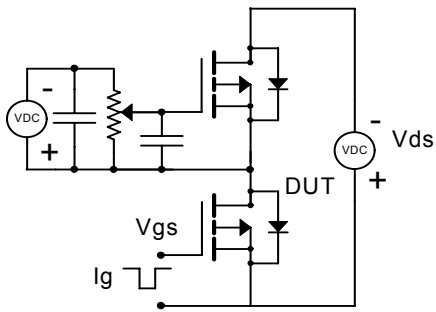
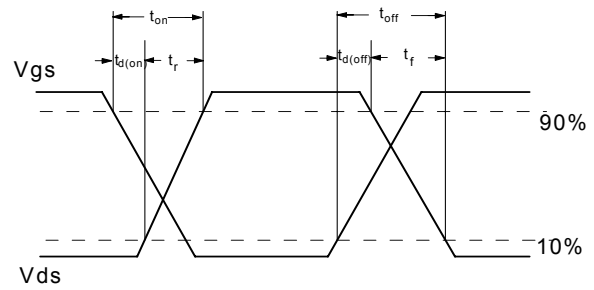
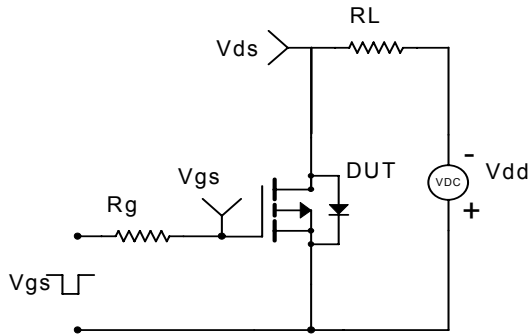


Figure 11: Normalized Maximum Transient Thermal Impedance

Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

